That which is claimed is:

1. A high power, high frequency semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a controlling electrode and first and second controlled electrodes; and

a thermal spacer dividing at least one of the unit cells into a first active portion and a second active portion, spaced apart from the first potion by the thermal spacer, the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the first thermal spacer.

2. The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer comprises a first thermal spacer, the semiconductor device further comprising a second thermal spacer that divides the at least one unit cell into a third active portion, the third active portion being spaced apart from the first and second active portions and the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the second thermal spacer.

3. The high power, high frequency semiconductor device of Claim 2, further comprising a third thermal spacer dividing an adjacent unit cell into a first active portion and a second active portion, the controlling electrode and the first and second controlled electrodes of the adjacent unit cell extend across the third thermal spacer and wherein the third thermal spacer is offset from the first and second thermal spacers.

4. The high power, high frequency semiconductor device of Claim 1, wherein the first and second active portions of the at least one unit cell comprise mesas and wherein the thermal spacer comprises a region between the mesas.

5. The high power, high frequency semiconductor device of Claim 4, wherein at least one of the first and/or second controlled electrodes of the at least one unit cell includes an air bridge across the region between the mesas.

6. The high power, high frequency semiconductor device of Claim 4, wherein the controlling electrode of the at least one unit cell is provided on sidewalls of the mesas and extends onto a floor of the region between the mesas.

7. The high power, high frequency semiconductor device of Claim 4, wherein the mesas comprise epitaxial layers on a substrate and wherein the region between the mesas comprises an exposed region of the substrate.

8. The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer comprises an electrically inactive implanted region and/or an insulator region between the first and second active portions of the at least one unit cell.

9. The high power, high frequency semiconductor device of Claim 1, wherein a cross-sectional area of the controlling electrode is greater where the controlling electrode crosses the thermal spacer than a cross-sectional area of the controlling electrode on the first and second active portions of the at least one unit cell.

10. The high power, high frequency semiconductor device of Claim 1, wherein a width of the controlling electrode is greater where the controlling electrode crosses the thermal spacer than a width of the controlling electrode on the first and second active portions of the at least one unit cell.

11. The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer is configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

12. The high power, high frequency semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arranged in a linear array.

13. The high power, high frequency semiconductor device of Claim 1, wherein the controlling electrode comprises a gate finger and the first and second controlled electrodes comprise source and drain electrodes.

14. The high power, high frequency semiconductor device of Claim 13, wherein the unit cells comprise unit cells of a silicon carbide MESFET.

15. The high power, high frequency semiconductor device of Claim 13, wherein the unit cells comprise unit cells of a GaN transistor.

16. The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer comprises an electrically inactive region configured so as to not generate heat when the semiconductor device is in operation.

17. A high power, high frequency field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region;

a plurality of gate electrodes of the unit cells, the plurality of gate electrodes being electrically connected in parallel;

a plurality of source electrodes of the unit cells, the plurality of source electrodes being electrically connected in parallel;

a plurality of drain electrodes of the unit cells, the plurality of drain electrodes being electrically connected in parallel; and

a plurality of thermal spacers that divide corresponding ones of the plurality of unit cells into at least a first active portion and a second active portion and wherein the gate electrodes, source electrodes and drain electrodes of the unit cells cross over the corresponding thermal spacers.

18. The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a linear array of unit cells.

19. The field effect transistor of Claim 17, wherein the plurality of thermal spacers provide a checkerboard pattern.

20. The field effect transistor of Claim 17, wherein the plurality of thermal spacers are substantially uniform in size.

21. The field effect transistor of Claim 17, wherein the plurality of thermal spacers are aligned between adjacent unit cells.

22. The field effect transistors of Claim 17, wherein the plurality of thermal spacers are non-uniform in size.

23. The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a plurality of silicon carbide unit cells.

24. The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a plurality of gallium nitride based unit cells.

25. The field effect transistor of Claim 17, wherein the first and second active portions of the unit cells comprise mesas and wherein the thermal spacers comprise regions between the mesas.

26. The field effect transistor of Claim 25, wherein a least one of the first and/or second controlled electrodes of the unit cells includes an air bridge across the region between the mesas.

27. The field effect transistor of Claim 25, wherein the controlling electrodes of the unit cells are provided on sidewalls of the mesas and extend onto floors of the region between the mesas.

28. The field effect transistor of Claim 25, wherein the mesas comprise epitaxial layers on a substrate and wherein the regions between the mesas comprise exposed regions of the substrate.

29. The field effect transistor of Claim 17, wherein the thermal spacers comprise an electrically inactive implanted region and/or an insulator region between the first and second active portions of the unit cells.

30. The field effect transistor of Claim 17, wherein a cross-sectional area of the controlling electrodes is greater where the controlling electrodes cross the

thermal spacers than a cross-sectional area of the controlling electrodes on the first and second active portions of the unit cells.

31. The field effect transistor of Claim 17, wherein a width of the controlling electrodes is greater where the controlling electrodes cross the thermal spacers than a width of the controlling electrodes on the first and second active portions of the unit cells.

32. The field effect transistor of Claim 17, wherein the thermal spacers are configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

33. The field effect transistor of Claim 17, wherein the thermal spacers comprise an electrically inactive region so as to not generate heat when the field effect transistor is in operation.